DOCUMENT RESUME

ED 050 579 EM 008 939

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TITLE	The PLATO IV Architecture.
INSTITUTION	Illinois Univ., Urbana. Computer-Based Education Lab.
SPONS AGENCY	Joint Services Electronics Program, Fort Monmouth, N.J.; Office of Education (DHEW), Washington, D.C.
REPORT NO	CERL-X-20
PUB DATE	Apr 71
CONTRACT	OEC-6-10-184
NOTE	20p.
EDRS PRICE	EDRS Price MF-$0.65 HC-$3.29
DESCRIPTORS	Cable Television, *Computer Assisted Instruction, Computers, Computer Storage Devices, *Digital Computers, Electronic Equipment, Information Processing, *Input Output Analysis, *Input Output Devices, Programing, *Telephone Communication Systems
IDENTIFIERS	PLATO IV, *Programed Logic for Automated Teaching Operation

ABSTRACT

The PLATO IV computer-based instructional system consists of a large scale centrally located CDC 6400 computer and a large number of remote student terminals. This is a brief and general description of the proposed input/output hardware necessary to interface the student terminals with the computer's central processing unit (CPU) using available transmission techniques, i.e., dedicated telephone lines and cable television (CATV) lines. The output controller is basically a parallel to serial converter which accepts data from the computer and encodes the data into a form compatible with the requirements of commercial CATV equipment. The input controller scans incoming lines from the terminals for data and controls the flow of that data to the computer. A peripheral processing unit controls the operation of the input controller with external function codes. A keyset multiplexor allows up to 32 PLATO IV terminals to share a common data line to the computer. (Author/JY)

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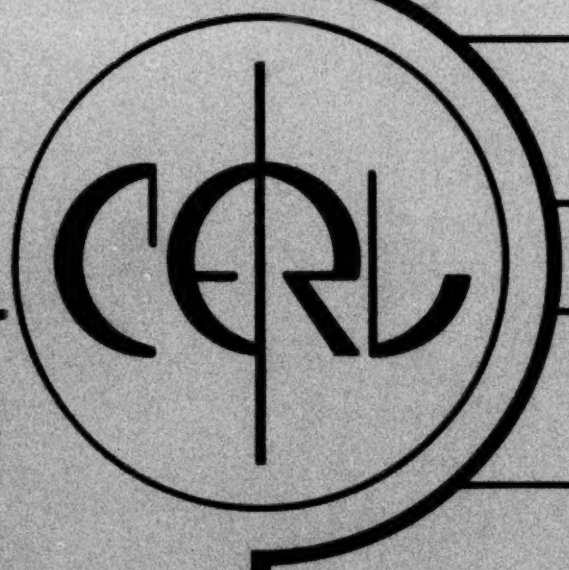
CERL REPORT X-20 APRIL, 1971

THE PLATO IV ARCHITECTURE

JACK STIFLE



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This work was supported by the National Science Foundation under Contract NSF GJ 81 and NSF GJ ~~947~~ 974.

PLATO has been supported by the Advanced Research Projects Agency through the Office of Naval Research Under Contract Nonr 3985(08), in part by the Joint Services Electronics Program (U.S. Army, U.S. Navy, and U.S. Air Force), in part by the Public Health Service, Division of Nursing of the U.S. Department of Health, Education and Welfare under Contract NPG-188-01, and in part by the U.S. Office of Education under Contract OE-6-10-184.

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A project of the size of PLATO IV necessarily requires the talents of many people only a few of whom are mentioned here.

Paul Tucker and Mike Johnson assisted in the design of the Network Interface Unit.

Len Hedges, Fred Holy, Jim Knoke, and Rich Slavens all contributed to the actual fabrication of the system hardware.

Thanks also to Jean Ciesa and Terry Gabrielse for their help in the assembly and typing of this report.

ABSTRACT

This report provides a general description of the hardware for the PLATO IV system. The various system components are identified and their functions described. Some programming information relating to the control of data in the PLATO network is also included.

The PLATO IV Architecture

by

Jack Stifle

Computer-based Education Research Laboratory

Introduction

This report is intended to serve as a brief and general description of the hardware for the PLATO IV system as it is presently envisaged. The function of the various systems components is described. A detailed description of the student terminal may be found in reference (1) and a more general description of the entire PLATO program may be found in reference (2).

System Description

A block diagram of a typical PLATO IV system is shown in Figure 1. Operation of the entire system is under control of a large scale centrally located computer. The Network Interface Unit supervises the flow of data between the computer and the PLATO network.

Data is distributed to the terminals in the system over a standard commercial television channel using a synchronous time division multiplex technique.[3] The data is transmitted over a leased cable television (CATV) facilities and is distributed in a manner similar to the distribution of commercial CATV signals. Data from the terminals is returned to the computer over dedicated voice grade (Schedule 4) telephone lines.

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[1] J. Stifle, "A Plasma Display Terminal," CERL Report X-15, March, 1970.

[2] D. Alpert and D. Bitzer,"Advances in Computer-based Education: A Progress Report on the PLATO System." CERL Report X-10 (Computer-based Education Research Laboratory, University of Illinois) July, 1969.

[3] J. Stifle, D. Bitzer, M. Johnson, "Digital Data Transmission Via CATV," CERL Report in preparation.

Most of the terminals in a PLATO system are grouped into classroom sites of up to 32 terminals each as shown in Figure 2. Data from these sites is returned directly to the Input Controller in the Network Interface Unit. Data from individual remotely located terminals is returned to the Concentrator. The Concentrator controls the flow of data from up to 32 terminals into the Input Controller.

Each PLATO classroom site contains:

- A Digital Television Receiver and Distributer (DTR)
- A Keyset Multiplexor (KST MPX)
- Up to 32 Student Terminals

The DTR unit recovers the data from the television channel and distributes it serially to the terminals over twisted pair lines at a rate of approximately 1200 bits/second.

The KST MPX transmits keyset data from the terminals to the computer over a voice grade phone line. The data from up to 32 terminals is transmitted over a single line in an asynchronous time division multiplex mode at a rate of 1200 bits/second.

The PLATO network can also provide service to individual remotely located terminals as shown in Figure 3. Data for such terminals is transmitted over voice grade phone lines which are connected to the output of a DTR unit. This DTR is identical with the DTR used in a classroom site and can be located anywhere in the PLATO network. Keyset data from individual terminals is returned directly to the computer center over a separate voice grade line.

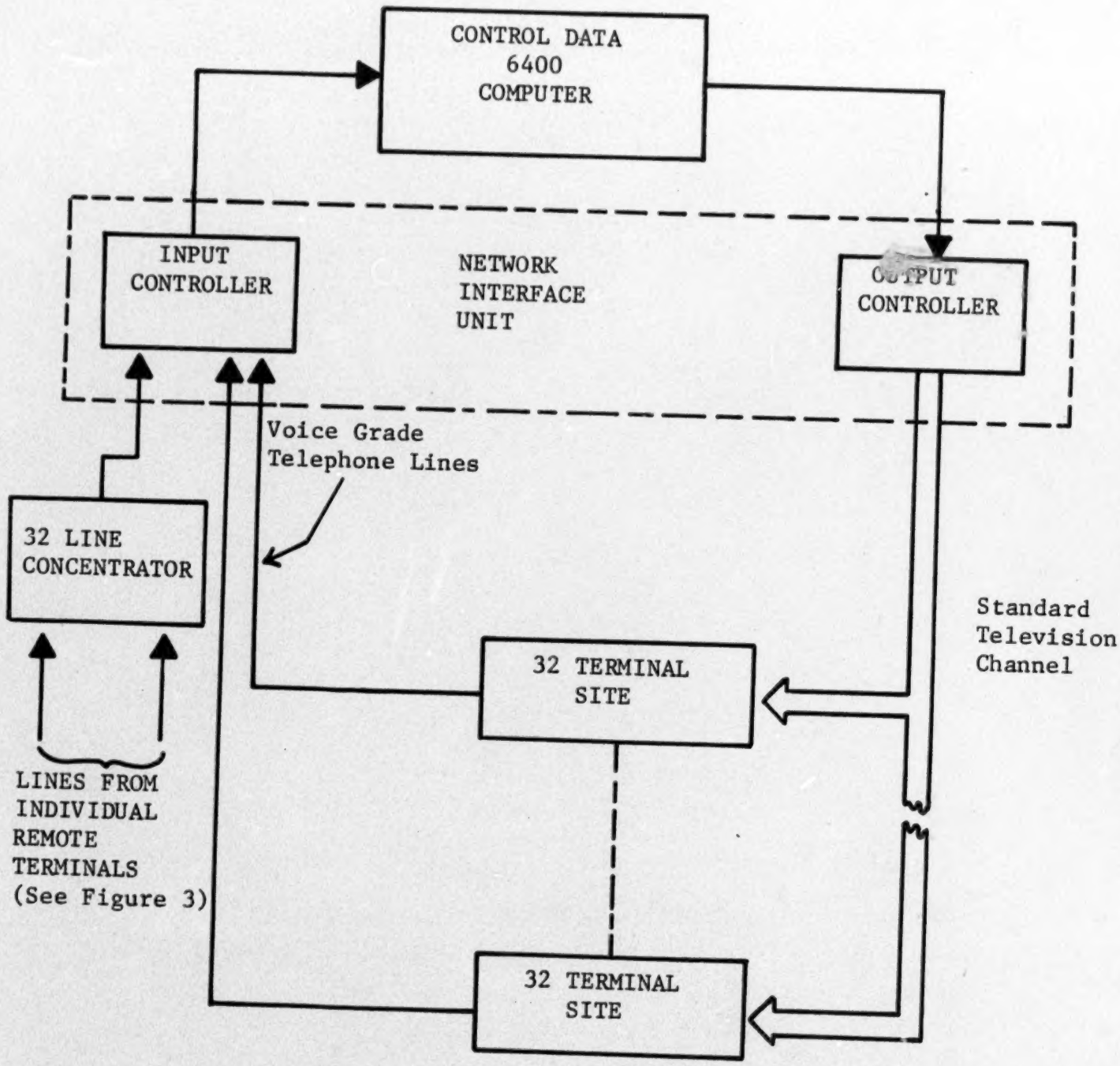

FIGURE 1 PLATO IV

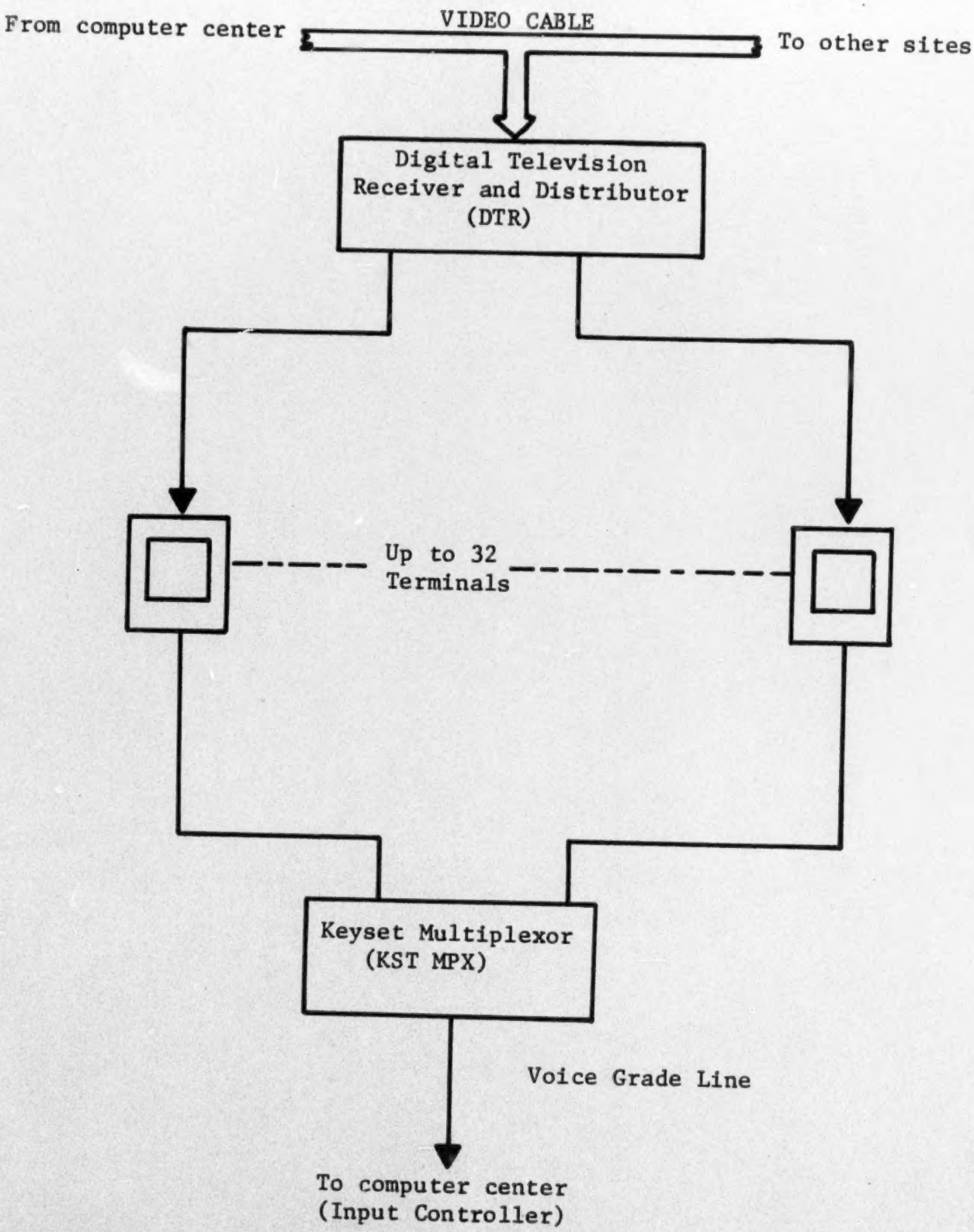

FIGURE 2 TYPICAL SITE CONFIGURATION

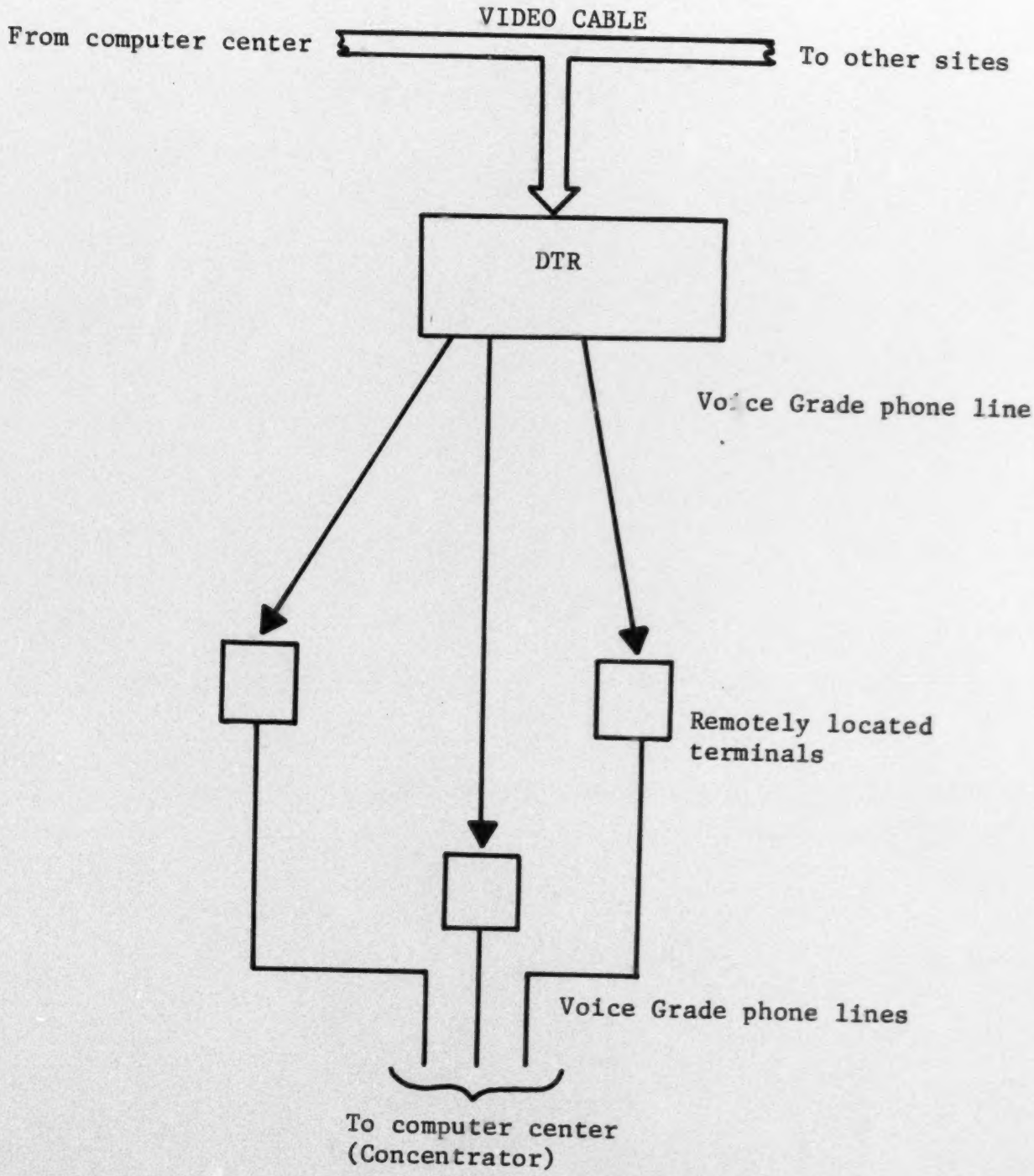

FIGURE 3 SINGLE TERMINAL SERVICE

Central Computer

Operation of the entire PLATO IV system is under control of a CDC 6400 computer system. This computer, see Figure 4, is a large scale general purpose computer containing one very fast central processing unit (CPU) and 10 independent peripheral processing units (PPU) which communicate with the CPU via the central memory. Augmenting the central memory is the extended core storage (ECS) system which can provide storage of up to two million additional words.

To operate a 1000 terminal PLATO system requires a 6400 with 65K words of central memory augmented by 500K words of ECS. With the addition of a second CPU and an additional 500K of ECS a PLATO system could be expanded to 2000 terminals.

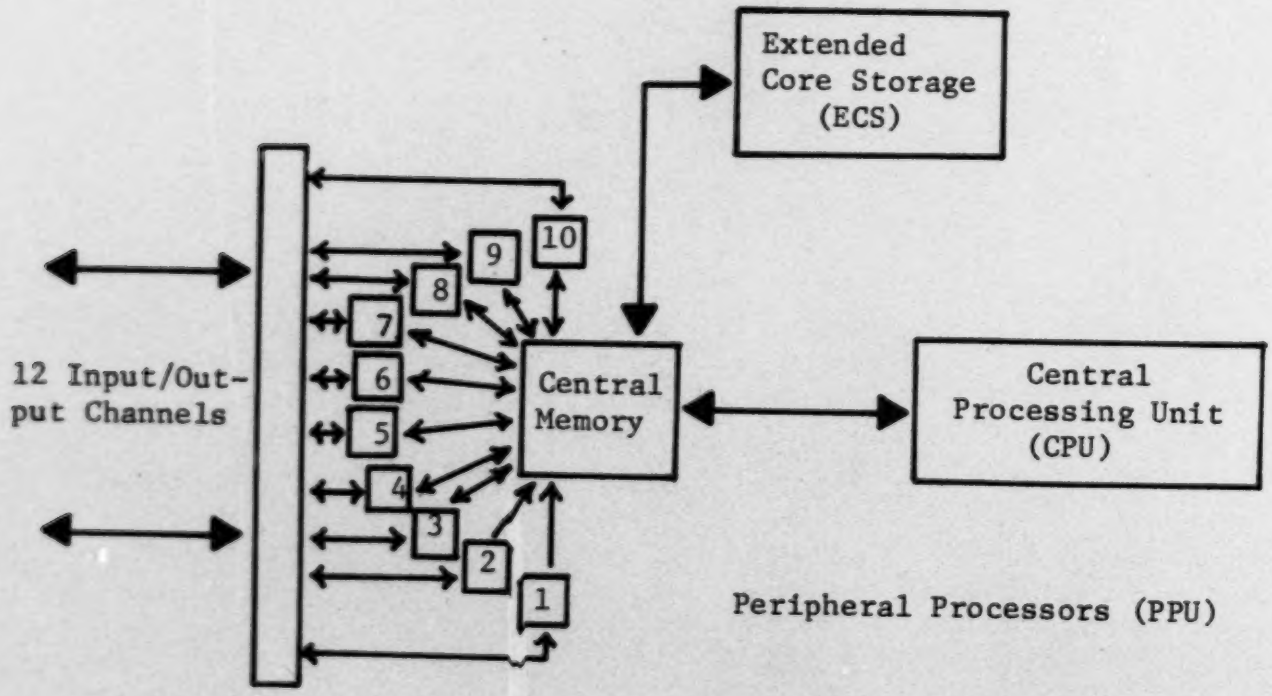

FIGURE 4 CDC 6400 COMPUTER

Network Interface Unit -- Output Controller

The Output Controller is basically a parallel to serial converter. This equipment accepts data from the computer and prepares it for transmission over the PLATO network.

A functional block diagram of the output controller is shown in Figure 5. The controller consists of two 1024 by 20 bit memories, a word assembly register, a write control, a read control, a four bit memory buffer register, a four bit shift register, and a digital data transmitter (DTX). The DTX encodes the data into a form compatible with the requirements of commercial cable television (CATV) equipment.[3] Requirements imposed by the DTX limit to 1008 the number of memory locations that may be used in either memory. Hereafter, then, the "contents" of a memory shall refer to the first 1008 locations of that memory.

The contents of either of the memories in the controller are loaded or read in 1/60 second. One memory is loaded by the computer during the 1/60 second that the other memory is being read into the DTX.

Each group of three 12 bit words from the computer is asembled by the Output Controller into one 30 bit word as shown in Figure 6.

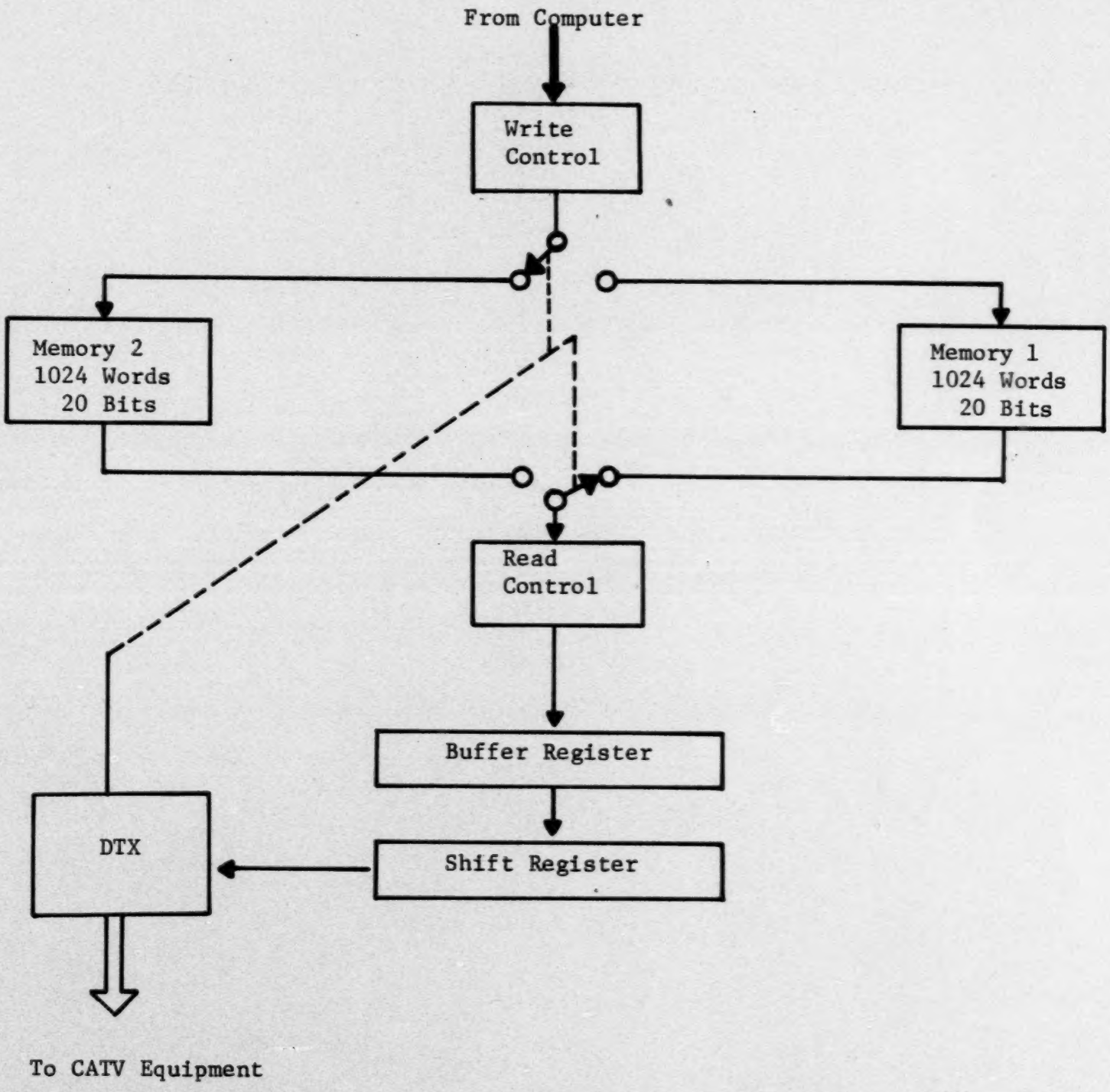

FIGURE 5 OUTPUT CONTROLLER - BLOCK DIAGRAM

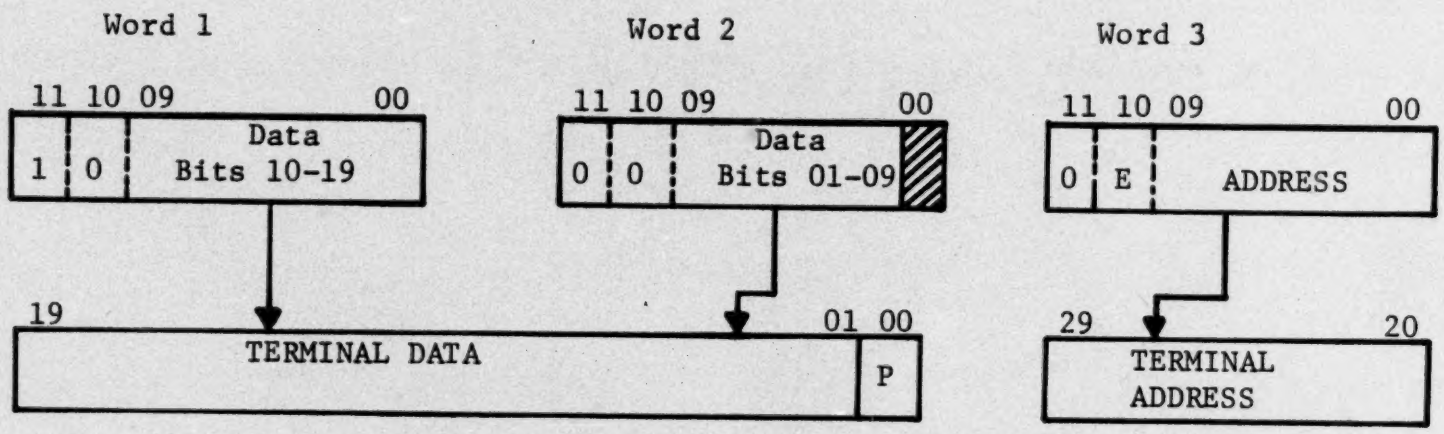

FIGURE 6 OUTPUT DATA FORMAT

Bit 00	Parity Bit. This bit is filled by the controller with a parity bit (odd parity) for the data portion of the word.
Bits 01-19	Terminal Data
Bits 20-29	Address of terminal for which data is intended.

Bits 10-11 of the three 12 bit words are control bits used by the controller as follows:

Bit 11, word 1	This bit indicates the first word of a 3 word sequence.
Bit 10, word 3	This bit, when equal to "1" indicates that this word is the address of the last terminal to receive data during the present 1/60 of a second.

Write (load) operations consist of storing the terminal data portions of the data words in a memory using the terminal addresses as memory addresses. Thus, for example, the data for terminal 355 would be stored in memory location 355. Parity bit assignment on the data is made just prior to the time the data is stored in memory.

A read operation consists of:

1. Read one bit from each of four consecutive memory addresses.
2. Load the four bits into the memory buffer register.
3. Write logical zeros in memory in place of the data.
4. Load the shift register from the buffer register.
5. Shift data from register to DTX.
6. Increment memory address.
7. After 1008 addresses are read, decrement the bit count.

Read operations continue until all 20 bits of all (1008) locations have been read and transmitted. After having been read the contents of each memory location is all "0"'s. An all "0"'s data word is interpreted by the PLATO IV terminals as a no-operation (NOP) code.[1] The computer is therefore required to send data only to those terminals requiring new information; the controller will automatically transmit NOP codes to all other terminals.

Network Interface Unit - Input Controller

All incoming lines from the PLATO IV terminals are routed to the input controller. The input controller scans these lines for data and controls the flow of the data into the peripheral processor.

The format of the incoming data is shown in Figure 7.

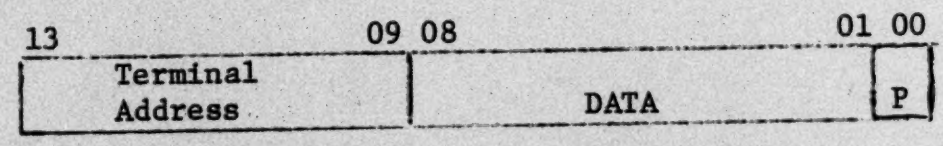

FIGURE 7 INPUT DATA FORMAT

Bit 00 Parity Bit

Bits 01-08 Data

Bits 09-13 Address of terminal sending data

A functional block diagram of the Input Controller is shown in Figure 8. The data on each line arrives at the controller at a rate of 1200 bits/ second and in the form of a frequency modulated (FM) signal. The demodulators recover the data from the fm signal and stores it temporarily in a holding register until it is read by the controller.

The controller is basically a 32 channel (14 bits/channel) multiplexor. The scanner scans the holding registers in the demodulators; if a register contains data the scanner halts, transfers the data to the peripheral processor and then resumes the scan. The scanner and computer operate at a rate sufficient to ensure that no data is lost on any incoming line. The Input Controller attaches a 5 bit channel address to the data word and checks the parity before sending the data on to the computer. The complete input data word, Figure 9, is disassembled into two 12 bit words for transmission to the computer.

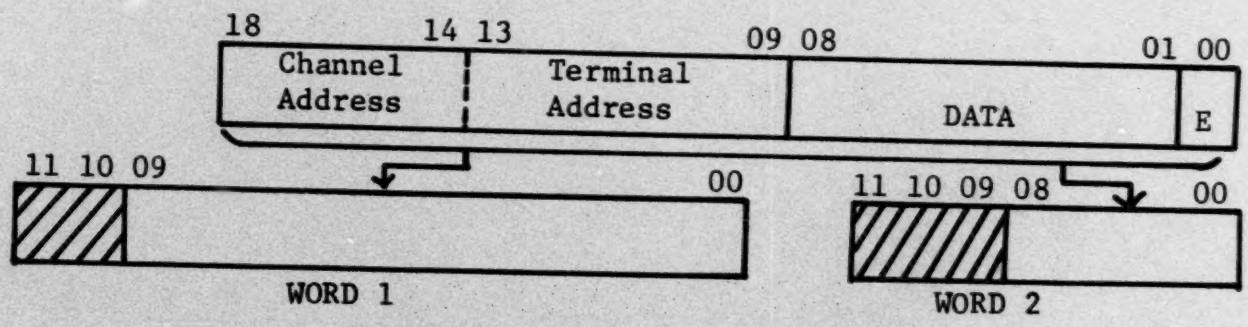

FIGURE 9 INPUT DATA WORD FORMAT

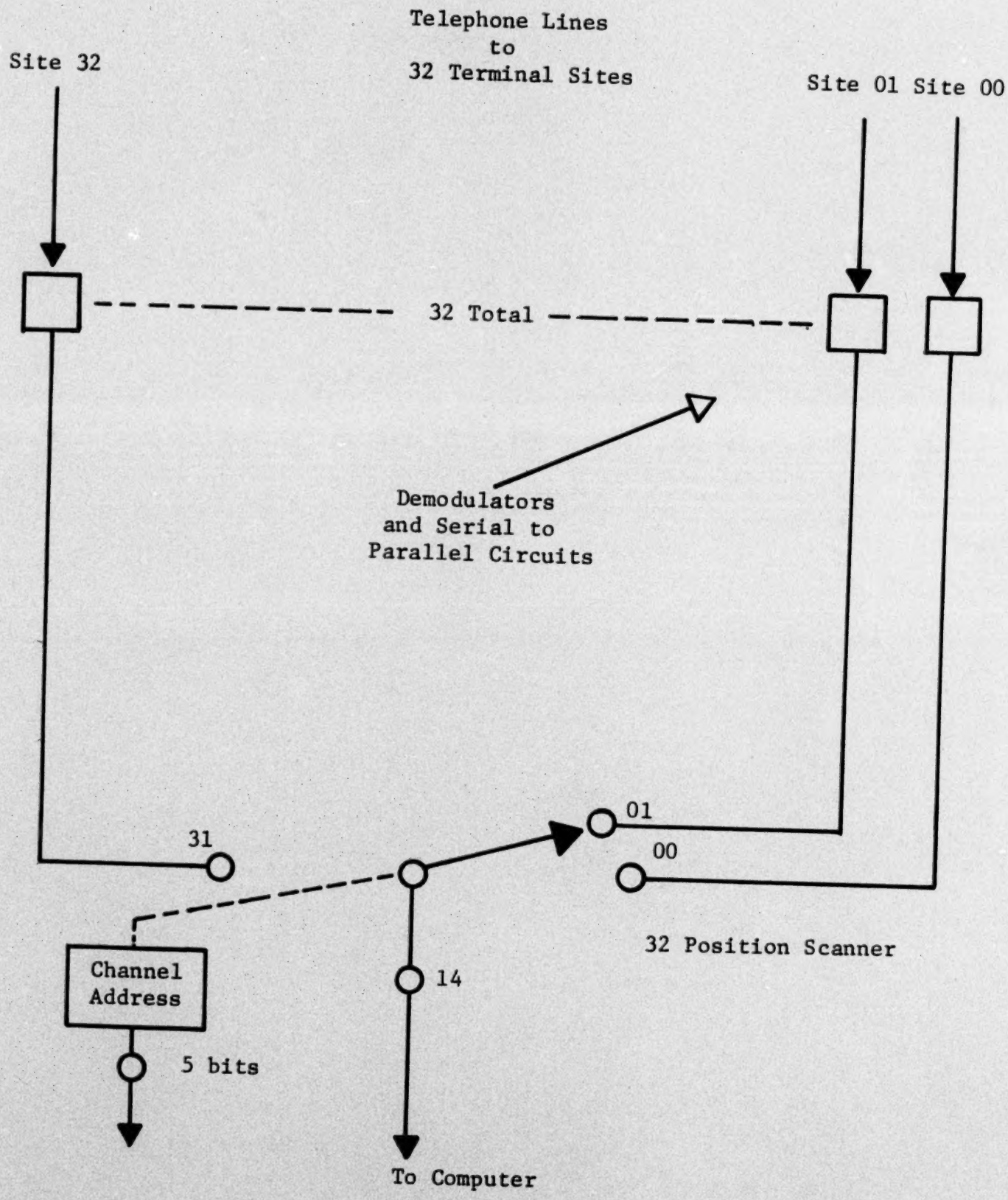

FIGURE 8 INPUT CONTROLLER - BLOCK DIAGRAM

Bit 00	Error Bit. If this bit is a 1, the data word contains an error.
Bits 01-08	Terminal Data.
Bits 01-13	Terminal Address.
Bits 14-18	Scanner Channel Address.

Input Controller Programming

The PPU controls the operation of the Input Controller with the external function (EXF) codes. These codes can be used to activate or deactivate any of the data lines arriving from the PLATO network. Status Request codes are also available for sensing the state of any of the data lines. The format of the EXF codes is shown in Figure 10.

Table 1 lists the function and Status Codes for the Output Controller. Each code is described below:

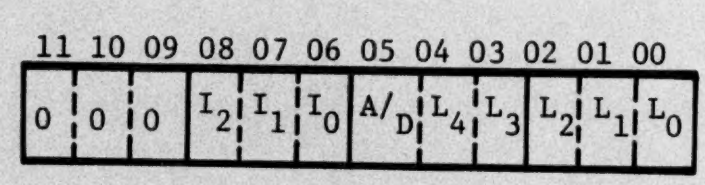

FIGURE 10 EXF FORMAT

Bits 00-04	Specify a scanner channel address.
Bit 05	Specifies an activate (Bit 5=1) or deactivate (Bit 5=0) function.
Bits 06-08	Specify function as follows: 000 - All channel function 001 - Single channel function 111 - Status Request Code
Bits 09-11	These bits specify the equipment number assigned to the Input Controller. They are always 0.

PLATO IV Input Controller EXF Codes

Function Code		
000 000 0 00000	Deactivate	All Channels
000 000 1 00000	Activate	All Channels
000 001 0 XXXXX	Deactivate	Channel XXXXX
000 001 1 XXXXX	Activate	Channel XXXXX
000 111 0 XXXXX	Sense	Inactive
000 111 1 XXXXX	Channel XXXXX	Active
x x x 0	Negative	Response to
x x x 1	Positive	Sense Codes

TABLE 1

Deactivate all lines (0000)

This code deactivates all channels.

Activate all lines (0040)

This code activates all channels.

Deactivate Channel (0100 - 0137)

These codes deactivate the channel specified by the lower five bits of the EXF code.

Activate Channel (0140 - 0177)

These codes activate the channel specified by the lower five bits of the EXF code.

Status Request Codes (0700 - 0777)

These codes may be used to sense the status of the Output Controller. A one word input must follow the Status Request to read in the status word. The status word has the format shown in Figure 11.

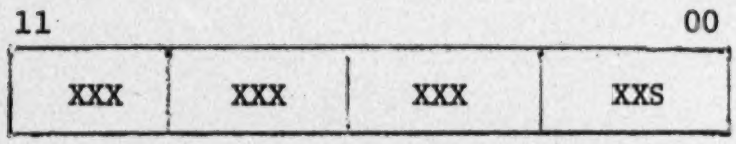

FIGURE 11 STATUS WORD FORMAT

Bit 00 — Sense Response. Bit 0='0' for a negative or a "1" for a positive response to the condition sensed for.

Bits 01-11 — Not used.

Keyset Multiplexor

This equipment permits up to 32 PLATO IV terminals to share a common data line to the computer center. A block diagram of the multiplexor is shown in Figure 12.

Each terminal sends data to the multiplexor on an 8 bit parallel channel. A scanner within the multiplexor scans these 32 channels for data. If data is present on a channel, the scanner halts and the data along with the address of that channel is placed in a 14 bit shift register. A parity bit is assigned and the data is then transmitted on to the computer center on a telephone line. The scanner operation is then resumed. The data format is as shown in Figure 8.

The data is encoded by the modulator as a frequency-modulated (fm) signal and transmitted at a rate of 1200 bps. Data rates per terminal range from 2-1/2 characters (8 bit/character) per second with all 32 terminals transmitting to 80 characters per second with 1 terminal transmitting.

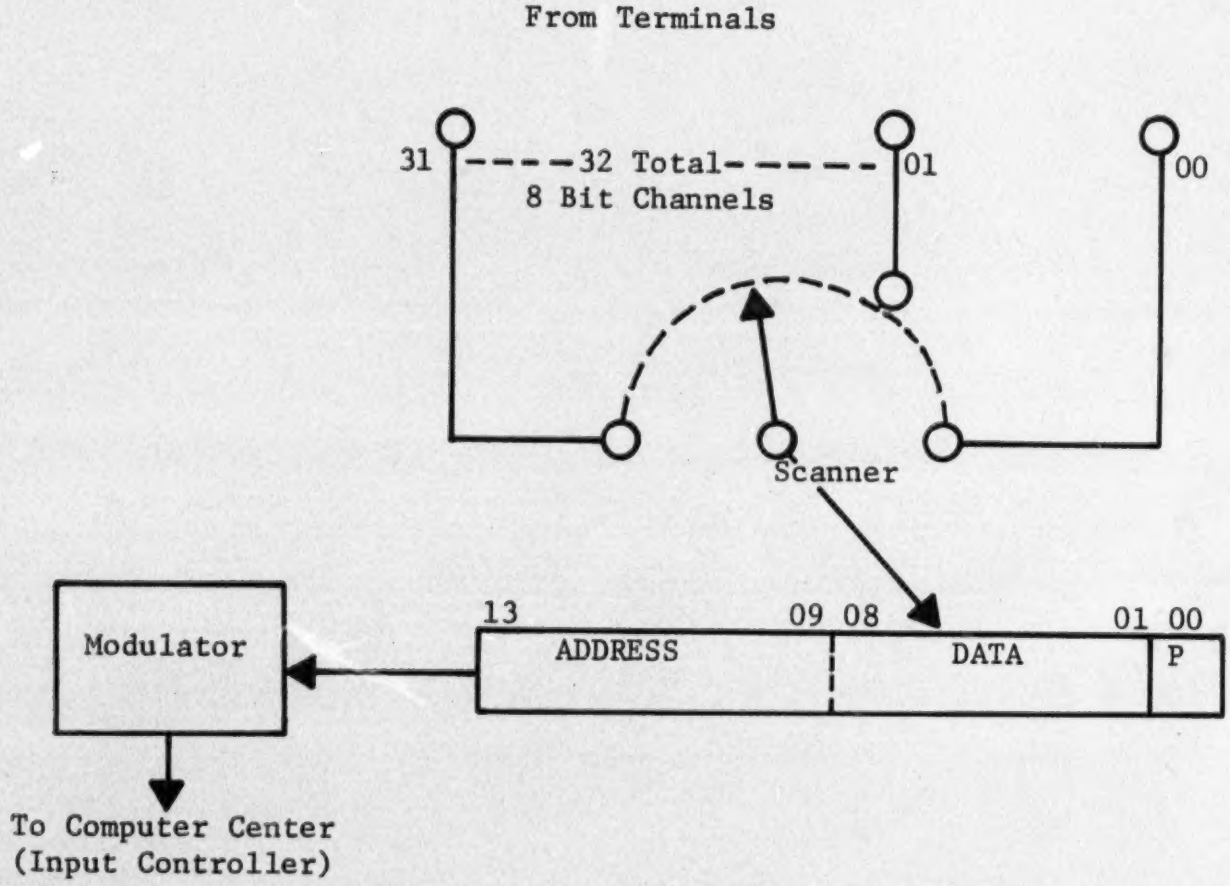

FIGURE 12 KEYSET MULTIPLEXOR